REMARKS

Claims 7-11 were examined. Claim 7 is amended. Claims 7-11 remain in the application.

The Patent Office rejects claims 7-11 under 35 U.S.C. §102(b) as anticipated by U.S. Patent No. 5,142,639 of Kohyama, et al. (Kohyama). The Patent Office rejects claim 11 under 35 U.S.C. §103(a) as obvious over Kohyama in view of KR 2001036045A of Choi, et al. (Choi). The rejection under 35 U.S.C. §103(a) is identified as the rejection of claims 7-10. However, the Patent Office directs its discussion only to claim 11. Accordingly, Applicants address the 35 U.S.C. §103(a) rejection as that of only claim 11.

Kohyama is cited for disclosing, among other things, a MIM capacitor in a via that conforms to a side wall of the via. Referring to Figure 2H of Kohyama, Kohyama identifies its MIM capacitor as including at least the unit stack of first insulation film 15, lower capacitor electrode 19, capacitor gate insulation film 20, upper capacitor electrode 21, another capacitor gate insulation film 20 and extension of lower capacitor electrode 19. See Kohyama at col. 3, lines 12-24 and Figure 2H. As shown in Figure 2H, upper capacitor 21 fills via 18 of the structure.

Choi is cited for ALCVD method to deposit a capacitor electrode in a via.

Claims 7-10 are not anticipated by Kohyama, because Kohyama does not describe a method including forming a via having a corrugated side wall; forming a decoupling capacitor stack in the via that conforms to the side wall of the via; forming a passivation layer on the decoupling capacitor stack; and forming a conductive material in the via, wherein the passivation layer is disposed between the conductive layer and the decoupling capacitor stack. Support for forming of a passivation layer and a conductive layer in the via may be found in the Application at, for example, paragraph [0025] as well as the actual process step described in reference to Figures 2-9. Kohyama defines it MIM capacitor to include electrode 21 that is separated from electrode 19 and fills via 18. Therefore, Kohyama does not describe forming a conductive material in the via wherein a passivation layer is disposed between a conductive layer in the via and a capacitor stack.

Applicants respectfully request that the Patent Office withdraw the rejection to claims 7-10 under 35 U.S.C. §102(b).

With respect to the rejection of claim 11 under 35 U.S.C. §103(a), claim 11 depends from claim 7 and therefore contains all the limitations of that claim. Claim 11 is not obvious over the cited references, because the references fail to disclose or provide any motivation, suggestion or prediction for forming a decoupling capacitor stack in the via; forming a passivation layer on the decoupling capacitor stack; and forming a conductive material in the via, wherein the passivation layer is disposed between the conductive layer and the decoupling capacitor stack. Combining the teachings of Choi and Kohyama, teaches the deposition of electrode material by ALCVD not each of the claimed forming operations embodied in claim 11.

Applicants respectfully request that the Patent Office withdraw the rejection to claim 11 under 35 U.S.C. §103(a).

CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

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Dated: 6/26/07

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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being transmitted by facsimile on the date shown below to the United States Patent and Trademark Office.

Nedy Calderon 6/26/07

Nedy Calderon Date